WHAT IS CLAIMED IS:

1. A logic simulation apparatus comprising:

extracting means for extracting clock domains and logic cones from a netlist representing connections among logic cells;

defining means for selecting and defining, as target portions to be speeded up, logic cones each of which carries out a logic operation in synchronization with one clock domain from the logic cones extracted by said extracting means, and for defining logic cones each of which carries out a logic operation based on a plurality of clock domains as nontarget portions not to be speeded up;

logic compressing means for compressing a logic of each of the target portions; and

verification means for performing a logic simulation on each of the target portions whose logic is compressed by said logic compressing means, and for performing a logic simulation on each of the nontarget portions.

2. The logic simulation apparatus according to Claim 1, wherein said verification means performs the logic simulation on each of the nontarget portions in consideration of at least one of (i) delay information about delays caused by the logic cells and delays caused by wires among the logic cells, and (ii) timing check information.

3. The logic simulation apparatus according to Claim 1, wherein said extracting means defines, as start points, primary inputs and data output points of the logic cells, also defines, as end points, primary outputs and data input points of the logic

cells, extracts a logical path from each of the start points to each of the end points, and integrates logical paths reaching an identical end point as one of the logic cones.

4. The logic simulation apparatus according to Claim 3, wherein said verification means performs a logic simulation on one of the nontarget portions adjacent to one of the target portions and connected to the data output point of one of the logic cells in consideration of the delay information about a delay caused by said one of the logic cells.

5. The logic simulation apparatus according to Claim 3, wherein said verification means performs a logic simulation on one of the nontarget portions adjacent to one of the target portions and connected to the data input point of one of the logic cells in consideration of the timing check information about said one of the logic cells.

6. The logic simulation apparatus according to Claim 1, wherein when performing a logic simulation on each of the target portions to be speeded up and also performing a logic simulation on each of the nontarget portions not to be speeded up, said verification means determines an output value of one of the logic cells receiving input data from the target portion and the nontarget portion in consideration of a logic value of each of the input data received by said one of the logic cells.

7. The logic simulation apparatus according to Claim 1, wherein when performing a logic simulation on each of the target portions to be speeded up and also performing a logic simulation

on each of the nontarget portions not to be speeded up, said verification means performs a timing check on each of data input from the target portion and the nontarget portion to one of the logic cells and assigns an unknown value to an output value of said one of the logic cells when detecting occurrence of a timing violation.